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Analysis of Cascaded Five Level Multilevel Inverter Using Hybrid Pulse Width Modulation

M. S. Sivagamasundari[1], Dr. P. Melba Mary[2]
[1]Assistant Professor, [2]Principal, Department of EEE, V V College of Engineering, Tisaiyanvilai

***Abstract*-- Multilevel inverter is an effective and practical solution for increasing power demand and reducing harmonics of AC waveforms. Such inverters synthesize a desired output voltage from several levels of dc voltages as inputs. This paper analyzes the performance of cascaded five level inverter using hybrid pulse width modulation technique. It has been found that this technique reduces the switching losses and total harmonic distortion. The topology used in this technique reduces the number of power switches when compared to the conventional cascaded H-bridge multilevel inverter. The performance has been analyzed by the MATLAB/Simulink. The output shows better performance results.**

***Keywords*-- Multilevel inverter, Cascaded H-Bridge multilevel inverter, Hybrid pulse width modulation, Total harmonic distortion.**

I. INTRODUCTION

A multilevel inverter is a power electronic converter that synthesizes a desired output voltage from several levels of dc voltages as inputs. With an increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multilevel inverter is their small output voltage, results in higher output quality, lower harmonic component, better electromagnetic compatibility, and lower switching losses. [1] [2].

High magnitude sinusoidal voltage with extremely low distortion at fundamental frequency can be produced at output with the help of multilevel inverters by connecting sufficient number of dc levels at input side. There are mainly three types of multilevel inverters; these are a) diode- clamped, b) flying capacitor and c) cascade multilevel inverter (CMLI).Among these three, the two most common topologies are the cascaded H-bridge inverter and its derivatives [3], and the Diode-clamped inverter [4]. The main advantage of both topologies is that the rating of the switching devices is highly reduced to the rating of each cell. However, they have the drawback of the required large number of switching devices which equals 2(*k*-1) where *k* is the number of levels. This number is quite high and may increase the circuit complexity, and reduce its reliability and efficiency. Cascaded H-bridge inverter has a modularized layout and the problem of the dc link voltage unbalancing does not occur, thus easily expanded to multilevel.

Due to these advantages, cascaded H-bridge inverter has been widely applied to such applications as HVDC, SVC, stabilizers, and high power motor drives. Diode clamped inverter needs only one dc-bus and the voltage levels are produced by several capacitors in series that divide the dc bus voltage into a set of capacitor voltages. Balancing of the capacitors is very complicated especially at large number of levels. Moreover, three-phase version of this topology is difficult to implement due to the neutral-point balancing problems. The output waveforms of multilevel inverters are in a stepped form, therefore they have reduced harmonics compared to a square wave inverter. To reduce the harmonics further, carrier-based PWM methods are suggested in the literature [5].

Several control and modulation strategies have been developed such as Multicarrier Pulse Width Modulation(PWM), Sinusoidal PWM, Space Vector PWM and Selective harmonic elimination. A cascaded hybrid multilevel inverter has been developed from a conventional cascaded multilevel inverter.

This paper analyzes the performance of cascaded five level inverter using hybrid pulse width modulation technique. It has been found that this technique reduces the switching losses and total harmonic distortion. The topology used in this technique reduces the number of power switches when compared to the conventional cascaded H-bridge multilevel inverter.

II. CASCADED FIVE LEVEL MULTILEVEL INVERTER

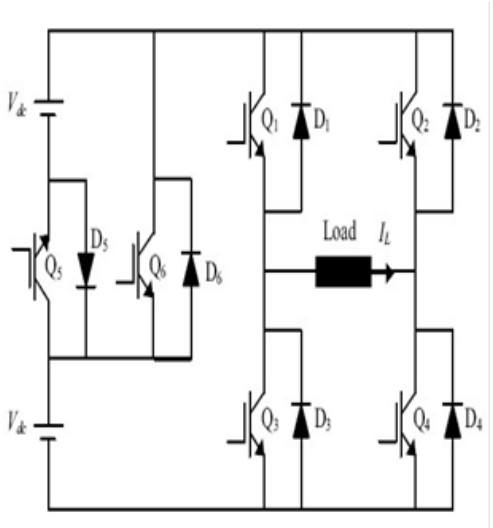

Fig.1.Single phase cascaded five level inverter

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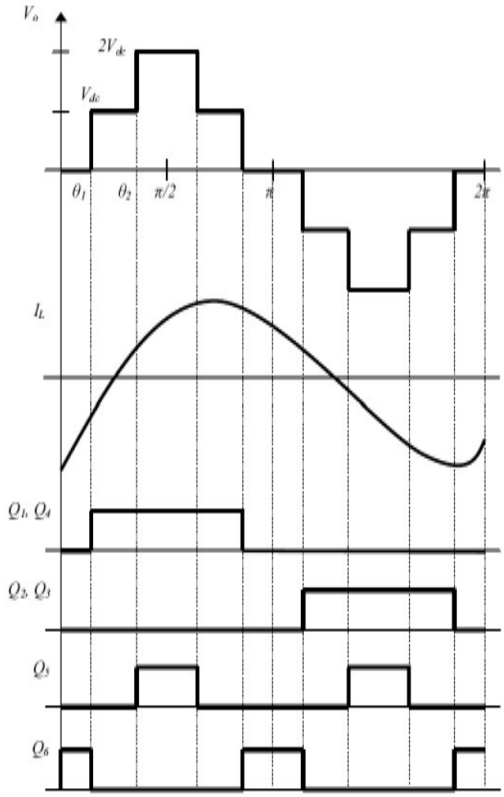

Fig.2.Waveforms of the proposed five level inverter topology

The single phase cascaded five level inverter topology has been proposed to reduce the number of power switches when compared to the conventional cascaded H-bridge multilevel inverter. A simplified single phase cascaded five level inverter topology is shown in Fig. 1. The circuit consists of four main switches in H-bridge configuration Q1~Q4, and two auxiliary switches Q5 and Q6. The number of dc sources (*two*) is kept unchanged as in similar 5-level conventional cascaded H-bridge multilevel inverter so that the output voltage of the cascaded multilevel inverter is V (t) = V1 (t) +V2 (t). Like other conventional multilevel inverter topologies, the proposed topology can be extended to any required number of levels. The inverter output voltage, load current, and gating signals are shown in Fig.2.[6]

III. Operation Of Single Phase Cascaded Five Level Inverter

The inverter can operate in three different modes according to the polarity of the load voltage and current. As these modes will be repeated irrespective of the number of the inverter levels, and for the sake of simplicity, the modes of operation will be illustrated for 5-level inverter, these modes are powering mode, free-wheeling mode and regenerating mode.[6]

1. Powering Mode

This occurs when both the load current and voltage have the same polarity. In the positive half cycle, when the output voltage is *Vdc*, the current pass comprises; the lower supply, D6, Q1, load, Q4, and back to the lower supply. When the output voltage is *2Vdc*, current pass is; the lower source, Q5, the upper source, Q1, load, Q4, and back to the lower source. In the negative half cycle, Q1 and Q4 are replaced by Q2 and Q3 respectively.[6]

2. Free-Wheeling Mode

Free-wheeling modes exist when one of the main witches is turned-off while the load current needs to continue its pass due to load inductance. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle current pass comprises; Q1, load, and D2 or Q4, load, and D3, while in the negative half cycle the current pass includes Q3, load, and D4 or Q2, load, and D1.[6]

3. Regenerating Mode

In this mode, part of the energy stored in the load inductance is returned back to the source. This happens during the intervals when the load current is negative during the positive half cycle and vice-versa, where the output voltage is zero. The positive current pass comprises; load, D2, Q6, the lower source, and D3, while the negative current pass comprises; load, D1, Q6, the lower source, and D4 . [6]

Table 1
Switching Strategy

Voltage	Q1	Q2	Q3	Q4	Q5	Q6
-Vdc	0	1	1	0	0	1
-0.5Vdc	0	1	1	0	0	0
0	1	0	0	1	0	1
0	0	1	1	0	1	0
0.5Vdc	1	0	0	1	0	0
Vdc	1	0	0	1	1	0

Table.1 shows the switching strategy for five level inverter.

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IV. HYBRID PWM TECHNIQUE

In PWM technique pulses of unequal widths are generated.

The pulse is generated by comparing a sinusoidal wave (modulating signal) of frequency 50HZ against a triangular wave (carrier signal). Each comparison gives one if the modulating signal is greater than the triangular carrier else zero. The number of pulses per cycle is decided by the ratio of the triangular carrier frequency to that of the modulating sinusoidal frequency.[7] From the Fig.1 the main inverter refers to H2 bridge and the auxiliary inverter refers to H1 bridge. Since the low switching losses during PWM operation is required, the main inverter will operate only at square wave mode and auxiliary inverter will operate at PWM mode. In practical, if a single chip is used to generate the PWM signals, it normally has only one carrier signal with six PWM channels; nevertheless, the hybrid multi level inverter requires 12 PWM channels for both main and auxiliary inverter. Thereafter, the referent signal of sinusoidal PWM (SPWM)used for the auxiliary inverter is modified by using equation (1)-(4).[7].

$$f(t)\ m\ Sin\ (t) \quad (1)$$

$$\frac{T_P}{T_C} = \begin{cases} 2\left(f(t) - \frac{1}{2}\right) ; \frac{1}{2} \le f(t) \le 1 \\ 2\left(\frac{1}{2} - f(t)\right) ; 0 \le f(t) \le \frac{1}{2} \end{cases} \quad (2)$$

$$A_1 = \begin{cases} 1 ; f(t) \ge 0 \\ 0 ; f(t) < 0 \end{cases} \quad (3)$$

$$A_2 = \begin{cases} 1 ; |f(t)| \ge \frac{1}{2} \\ 0 ; |f(t)| < \frac{1}{2} \end{cases} \quad (4)$$

where $f(t)$ is a referent signal,
m_a is modulation Index (0.0/1.0-1.0/1.0)
A_1 is a multiplexing signal #1,
A_2 is a multiplexing signals #2,
$\frac{T_P}{T_C}$ is pulse width of PWM (0.0–1.0).

V. SIMULATION RESULTS

In this paper, the simulation model is developed with MATLAB/SIMULINK. The simulation results of the proposed five level inverter is shown in Fig.3 and the corresponding FFT analysis is shown in fig 4. The generated output pulses from the pulse generator is shown in the Fig. 5 and those pulses generated are to drive the devices in to ON for a five level inverter topology.

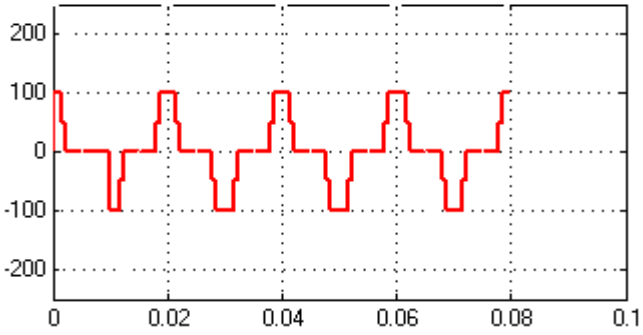

Fig. 3. Output Voltage for Five Level Inverter

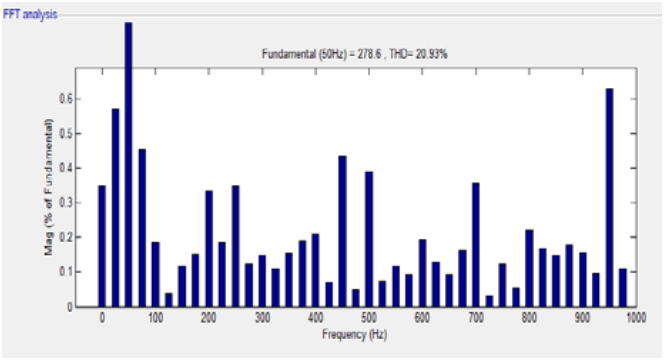

Fig. 4. FFT Analysis for Five Level Inverter

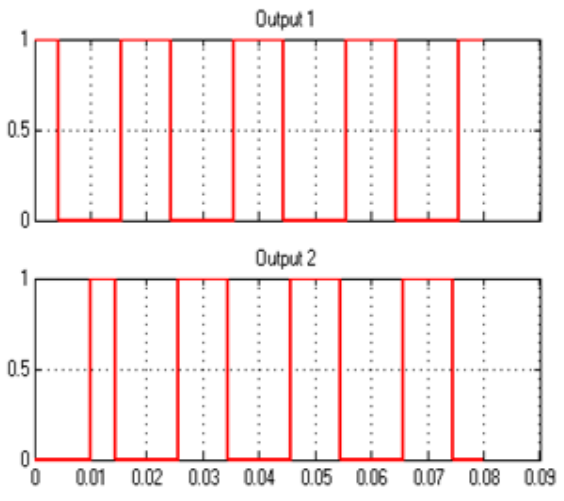

Fig.5. Generated gate pulses

VI. CONCLUSION

In the Present Work , performance of cascaded five level inverter using hybrid pulse width modulation technique has been analyzed**.** The topology used in this technique reduces the number of power switches and switching losses. In the conventional cascaded H-bridge multilevel inverter eight power switches have been used is reduced to six power switches by employing this topology and it can be employed for high voltage and high power applications. The performance has been analyzed by the MATLAB/Simulink. The simulation output shows very favourable result and shows a minimum total harmonic distortion of 20.94%.

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